REMARKS

Reconsideration and allowance of outstanding claims 1-43 in view of the following remarks are requested.

A. Claim Rejections under 35 USC §112

The Examiner has rejected claims 8, 11, 26, and 29, and their dependent claims stating that "the distinction between the conduction surface implant and the isolation surface implant is unclear." Applicant respectfully disagrees. The claimed phrases "conduction surface implant" and "isolation surface implant" are interpreted in light of the detailed description. In the detailed description, Applicant has stated the differences between the two throughout the detailed description and has illustrated same in the drawings. For example, the detailed description states: "In FIG. 4, two additional implants have been added to the semiconductor device 300 of FIG. 3, a conduction surface implant 405 and an isolation surface implant 410." Page 9, lines 15-16. As another example, in relation to the conduction surface implant, the detailed description states: "The conduction surface implant 405 is, in one example implementation, formed by implanting an N-type dopant (e.g. phosphorous) to overlie the photodiode 105." Page 9, lines 20-22.

In contrast, with respect to the isolation surface implant, the detailed description states: "In one example implementation, the isolation surface implant is formed by implanting a P-type dopant (e.g. boron) to overly the photodiode 105 where needed." Page 10, lines 10-12. As such, the two phrases "conduction surface implant" and

"isolation surface implant" are illustrated in the drawings, defined in the detailed description, and in fact are stated to be of two different dopant types in the exemplary embodiments disclosed. As such, Applicant respectfully submits that the Examiner's §112, second paragraph, rejection has been overcome.

B. Rejection of Claims under §102(e) and §103(a)

The Examiner has rejected claims 1-3, 5-16, 19-20, 26-33, 36-37 under 35 USC §102(e) as being anticipated by Suzuki et al (Pub. No. US 2001/0015435 A1) (hereinafter, "Suzuki"). The Examiner has separately rejected claims 4, 17-18, 21-25, 34-35, and 38-43 under 35 USC §103(a) as being unpatentable over Suzuki in view of Rhodes et al (Pub. No. US 2001/0017382 A1) (hereinafter, "Rhodes"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by independent claims 1, 26, 29, 32, and 36, is patentably distinguishable over Suzuki and Rhodes, either singly or in combination. However, Applicant reserves the right to provide declarations and/or documents under 37 CFR §1.131 to "swear behind" the respective effective filing dates of Suzuki and/or Rhodes.

Subject to Applicant's reserved right to establish priority of the present invention under 37 CFR §1.131, Applicant submits that the present invention, as defined by each independent claims 1, 26, 29, 32, and 36, teaches, among other things, a junction isolation region formed in the substrate, where the junction isolation region is formed between the photodiode and the trench isolation region, and where the junction isolation region

prevents contact between the photodiode and the trench isolation region. See independent claims 1, 26, 29, 32, and 36.

The present application is specifically directed to overcoming problems associated with use of trench isolation regions which in turn have been used in lieu of LOCOS isolation which is the basis for the Examiner's rejection of the present invention in view of Suzuki and/or Rhodes. The present application states, for example, that "One source of dark current is from the shallow trench isolation process methods for typical CMOS logic and analog process flows that have not yet been optimized for extremely low reverse bias junction leakage. As is well known in the art, shallow trench isolation is used for various metal oxide semiconductor circuits to address common problems associated with standard LOCOS isolation (e.g., bird's beak problems where oxide grows under the edge of the blocking silicon nitride layer to increase the size of the semiconductor device). In standard shallow trench isolation, a shallow trench is etched between elements in a semiconductor and filled with a deposited dielectric. After sidewall oxidation and dielectric fill of oxide, a CMP step typically occurs." Page 2, lines 11-20 (emphasis added).

Thus, as stated in the present application, the present invention is specifically directed to reducing "dark current" in image sensors that utilize shallow trench isolations as opposed to LOCOS isolation. The shallow trench isolation, as stated above, is formed by etching a trench and filling same, followed by a typical CMP (chemical mechanical polish) step. The invention specifically is directed to utilization of a shallow trench

process instead of using a LOCOS "local oxidation of silicon" process. The LOCOS oxide is a thick thermally grown field oxide which has been conventionally used, as disclosed in Suzuki and Rhodes. Thus, Suzuki and Rhodes are not even directed to a technique of reducing dark current in shallow trench isolation devices.

The present application further states: "The source of the dark current in shallow trench isolation methods for typical CMOS process flows usually stems from damage to the silicon surface that occurs during etching of the shallow trench. This damage increases the density of traps and other imperfections in the silicon substrate and causes increased junction leakage . . . ." Page 2, line 21 through page 3, line 1 (emphasis added). Thus, the dark current that is intended to be reduced by the present invention results from a damage unique to etching a shallow trench. In contrast, Suzuki and Rhodes do not disclose and are not event directed to overcoming dark current for CMOS sensors using a shallow trench isolation process, and the source of such dark current is lacking in a LOCOS process.

Furthermore, as seen in Figure 5 of Suzuki, the semiconductor well region 351 is formed beneath LOCOS 34 as a continuous, i.e. blanket, well region. See paragraph 0072 of Suzuki. However, the invention utilizes junction isolation regions 305 as a "ring" solely encircling trench isolation regions 210. See, for example, Figures 4 and 5 of the present application.

C. Conclusion

Based on the foregoing reasons, Applicants submits that independent claims 1, 26, 29, 32, and 36, and claims depending therefrom are distinguishable over Suzuki and Rhodes, either singly or in combination. Thus, Applicant respectfully requests an early allowance of claims 1-43 pending in the present application.

Please note that Applicant's attorneys have changed. Applicant has filed a "revocation and power of attorney" to formally effect this change. The contact information of Applicant's new attorneys appear below.

Respectfully Submitted,
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